Application No. 09/591,044
Filed: June 9, 2000
Group Art Unit: 2189

REMARKS

The instant Amendment is filed in response to the official action dated February 4, 2003. Reconsideration is respectfully requested.

Claims 1-9 are currently pending.

Claims 1-9 stand rejected.

Claims 1-4 and 6-9 have been amended to more distinctly claim the Applicants' invention.

The Examiner has rejected claims 1-2 and 5-7 under 35 U.S.C. 103(a) as being unpatentable over Trieu et al. in view of Carson et al. Specifically, the official action indicates that the Trieu reference does not teach the first device operative at least at the second clock rate to store at least a portion of the data in a register, and the second device operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device. The official action further indicates that the Carson reference teaches "operative at least at the second clock rate to store at least a portion of the data in a register (specification, column 5, line 61, to column 6, line 6), and operative at least at the second

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clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device (specification, column 8, lines 9-13)."

However, because there is no evidence of a suggestion, teaching, or motivation to combine the Trieu and Carson references (*e.g.*, the Trieu reference relates to the field of interfacing devices to a bus, while the Carson reference relates to the significantly different field of lighting controllers), the Applicants respectfully submit that the official action merely outlines an improper hindsight-based obviousness analysis, *i.e.*, the official action merely takes the Applicants' disclosure as a blueprint for piecing together the prior art to defeat patentability, which is the essence of hindsight (see *e.g.*, *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985)).

Even if there were sufficient evidence of a motivation to combine the Trieu and Carson references as suggested in the official action, the resulting combination would not meet the Applicants' claims. For example, the Carson reference fails to disclose the operation of driving the clock line to a first

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predetermined logic level (*e.g.*, a low logic level) while the data is stored in the register, as recited in amended claims 1 and 6. Specifically, the passage cited in the official action (*i.e.*, column 8, lines 9+, of Carson et al.) discloses, in relevant part, that each time a zero crossing signal makes a high to low transition, such as shown by the down directed arrows in Fig. 8 of the Carson reference, the remote input to the micro-controller is sampled to obtain the logic level. This passage further discloses that if the remote input is high, then the LSB for one remote input register is set to logic "1" - if the remote input is low when the zero crossing makes its high to low transition, then the LSB of the register is cleared to a "0".

However, the register **64**, as described above and disclosed in the Carson reference, does not function as a clock line, but instead functions as a shift register to hold the bits of a HEX encoded data word received over the remote input, for subsequent comparison with bits stored in a serial encoder register **70** (see column 6, lines 54+, and Fig. 3, of Carson et al.). Clearly, the LSB of the register **64** reset to a "0" cannot correspond to the clock line driven to the first predetermined logic level, as recited in amended claims 1 and 6.

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The Applicants further submit that the Carson reference neither teaches nor suggests driving the clock line to a first predetermined logic level while the data is stored in the register, in the event the at least one first device is operating at the second reduced clock rate, as recited in amended claims 1 and 6. This is because Carson does not deal with the problem of performing power management functions, *e.g.*, such functions involving the transfer of data via a bus whether or not one of the devices involved in the data transfer is "sleeping" (*i.e.*, operating in a reduced frequency or suspended power state). Instead, Carson addresses the significantly different problem of sending control signals from a controller to a plurality of dimmer switch stations independently of the line phase of power supplying each dimmer or controller (see column 4, lines 47-57, of Carson et al.). Moreover, the cited Trieu and Hamilton references fail to cure the deficiencies of the Carson reference. By driving the clock line to the first predetermined logic level while the data is stored in the register in the event the first device is operating at the second reduced clock rate, as recited in amended claims 1 and 6, data transfer between the first device and at

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least one second device on the bus is enabled while the first device operates at the reduced clock rate.

The Applicants therefore submit that even if the Trieu, Carson, and Hamilton references were combined in the manner suggested in the official action, the resulting combination would not meet amended base claims 1 and 6, and thus neither Trieu, Carson, nor Hamilton taken alone, nor any combination thereof, can render amended base claims 1 and 6 and the claims dependent therefrom obvious. Accordingly, the Applicants respectfully submit that the rejections of claims 1-9 under 35 U.S.C. 103(a) are unwarranted and should be withdrawn.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

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The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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--DRAFT--

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